PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2001-339057
(43)Date of publication of application : 07.12.2001

(51)Int.Cl. H01L 27/146
G06T 1/00
H01L 21/3205
H01L 21/768
H01L 27/00
H01L 21/8238
H01L 27/092
H01L 27/14
H01L 29/786
H04N 5/335

(21)Application number : 2000-160330
(22)Date of filing : 30.05.2000

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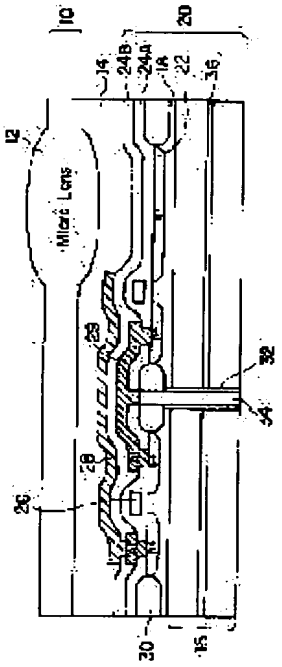
(54) METHOD OF MANUFACTURING THREE-DIMENSIONAL IMAGE PROCESSOR

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a manufacturing method for a three-dimensional image processor which can sharply simplify the manufacture process due to needlessness of mounting and removal process of a supporting board, can manufacture a three-dimensional image processor by simple and easy process, and can form embedded wiring surrounded by a highly reliable insulating film.
SOLUTION: A transparent substrate 10 made of quartz glass, where many microlenses 12 are made two-dimensionally, is bonded to a photoelectric transfer substrate 20 where a photodiode and a MOS transistor are made on an n-type silicon crystalline substrate 16 wherein an insulating layer 36 consisting of silicon diode is inserted, through an adhesive 14 consisting of high polymer material such as epoxy resin, polyimide resin, or the like, so that the main face of the photoelectric transfer substrate 20 and the rear of the transparent substrate 10 may oppose to each other.



LEGAL STATUS

[Date of request for examination] 19.04.2004

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or

application converted registration]
[Date of final disposal for application]
[Patent number]
[Date of registration]
[Number of appeal against examiner's decision of rejection]
[Date of requesting appeal against examiner's decision of rejection]
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CLAIMS

[Claim(s)]
[Claim 1] The manufacture approach of a three-dimension image processing system of pasting up the transparence substrate equipped with the lens which condenses light, and the photo-electric-conversion substrate which was electrically connected to this optoelectric transducer while the optoelectric transducer was formed in the principal plane and with which it embedded and wiring was formed so that the rear face of a transparence substrate and the principal plane of a photo-electric-conversion substrate may counter, and manufacturing a three-dimension image processing system.
[Claim 2] The manufacture approach of a three-dimension image processing system according to claim 1 of grinding the rear-face side of said photo-electric-conversion substrate, exposing said embedding wiring, pasting up so that the magnification conversion substrate which was electrically connected to this amplifier and the analog-to-digital converter and with which it embedded and wiring was formed may be electrically connected to the outcrop of said embedding wiring in this amplifier and an analog-to-digital converter while an amplifier and an analog-to-digital converter are formed in the rear face of this photo-electric-conversion substrate at a principal plane, and manufacturing a three-dimension image processing system.
[Claim 3] The manufacture approach of a three-dimension image processing system according to claim 2 of grinding the rear-face side of said magnification conversion substrate, exposing said embedding wiring, pasting up so that the data storage substrate which was electrically connected to this data storage while data storage was formed in the rear face of this magnification conversion substrate at the principal plane and with which it embedded and wiring was formed may be electrically connected to the outcrop of said embedding wiring in this data storage, and manufacturing a three-dimension image processing system.
[Claim 4] The manufacture approach of a three-dimension image processing system according to claim 3 of grinding the rear-face side of said data storage substrate, exposing said embedding wiring, pasting up so that the data-processing substrate which was electrically connected to this data processor while the data processor was formed in the rear face of this data storage substrate at the principal plane and with which it embedded and wiring was formed may be electrically connected to the outcrop of said embedding wiring in this data processor, and manufacturing a three-dimension image processing system.
[Claim 5] The manufacture approach of a three-dimension image processing system according to claim 4 of grinding the rear-face side of said data-processing substrate, exposing said embedding wiring, pasting up so that the output circuit substrate which was electrically connected to this output circuit while the output circuit was formed in the rear face of this data-processing substrate at the principal plane and with which it embedded and wiring was formed may be electrically connected to the outcrop of said embedding wiring in this output circuit, and manufacturing a three-dimension image processing system.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the manufacture approach of a three-dimension image processing system.
[0002]
[Description of the Prior Art] In recent years, development of the three-dimension semiconductor integrated circuit equipment which accumulated two or more circuit functional block in three dimensions is furthered from the purposes, such as high integration, densification, etc. of semiconductor integrated circuit equipment. Especially the three-dimension image processing system (intelligent image processor) that unified the digital disposal circuit for processing image sensors and its signal carries out high-speed processing of the image data obtained from a photosensor at juxtaposition, and since it becomes possible to obtain a high-definition image on real time, it has many hope.
[0003] Although the manufacture had been considered by the monolithic method which repeats SOI substrate formation and formation of the semiconductor device to a SOI substrate using the SOI (Silicon On Insulator) technique by laser recrystallization etc. at the beginning, these three-dimensions semiconductor integrated circuit equipment had problems, like production time with difficult crystalline reservation is long, in order to have carried out the laminating of the SOI to the multilayer.
[0004] For this reason, the manufacture approach of the three-dimension semiconductor integrated circuit equipment by the lamination technique which sticks the single crystal semiconductor substrates by which a semiconductor device or semiconductor integrated circuit equipment was produced beforehand is considered variously.
[0005] The CUBIC technique which sticks the semi-conductor substrate thin-film-ized by polish as a kind of a lamination technique on a monthly semiconductor world (1990 year 9 month number p58-64, such as wood Yoshihiro) is proposed. With a CUBIC technique, after pasting up the 1st semi-conductor substrate with which the semiconductor device was first formed on the silicon substrate on a support substrate, polishing of the excessive silicon substrate is carried out, and it is thin-film-ized. Next, wiring required for connection of the lengthwise direction of devices, such as embedding wiring, backwiring, and a contact member that consists of a bump/a pool, is formed, and the 1st semi-conductor substrate and the 2nd semi-conductor substrate with which the semiconductor device was formed on the silicon substrate are stuck. And finally a support substrate is removed and the semiconductor device of multilayer structure is completed.

[0006] Moreover, the manufacture approach of the three-dimension semiconductor integrated circuit equipment by the lamination technique is indicated by JP,6-260594,A. Although the point which carries out polishing of the excessive silicon substrate, and thin-film-izes it is common on the CUBIC technique after this approach pastes up the 1st semi-conductor substrate with which the semiconductor device was formed on the silicon substrate on a support substrate The point that the deep groove for forming embedding wiring in the 1st semi-conductor substrate beforehand is prepared, And it differs from the CUBIC technique at the point which removes a

support substrate for the 1st semi-conductor substrate and the 2nd semi-conductor substrate with which the semiconductor device was formed on the silicon substrate after lamination and lamination, and forms embedding wiring.
[0007]
[Problem(s) to be Solved by the Invention] However, any manufacture approach includes the process which exfoliates lamination in a support substrate, and exfoliates the 1st semi-conductor substrate from a support substrate in the 1st semi-conductor substrate after grinding, and had the problem that a production process was complicated. Since it is necessary to form the transparence substrate equipped with the micro lens which constitutes image sensors in the front face after removing a support substrate to manufacture a three-dimension image processing system especially, a production process becomes complicated still more.
[0008] Moreover, with a CUBIC technique, in order to remove a support substrate after carrying out polishing of the excessive silicon substrate and thin-film-izing it, when removing a support substrate, there was a problem that the integrated circuit formed on the semi-conductor substrate was damaged.
[0009] moreover, by the approach indicated by JP,6-260594,A In order to paste up the 1st semi-conductor substrate with which the deep groove for forming embedding wiring was prepared beforehand on a support substrate, In order to oxidize the side attachment wall of a deep groove and to form an insulator layer, after pasting up the problem that removal of the adhesives which entered the deep groove is difficult, and the 1st semi-conductor substrate and the 2nd semi-conductor substrate, Oxidation temperature could not be raised beyond the heat-resistant temperature of adhesives, but there was a problem that a reliable insulator layer could not be formed.
[0010] This invention is made in view of the trouble of the above-mentioned conventional technique, the purpose of this invention has the unnecessary attachment-and-detachment process of a support substrate, a production process can be simplified sharply, and it is in offering the manufacture approach of a three-dimension image processing system that a three-dimension image processing system can be manufactured according to a simple and easy process. Moreover, other purposes of this invention are to offer the manufacture approach of the three-dimension image processing system which was surrounded by the reliable insulator layer and which can embed and can form wiring.
[0011]
[Means for Solving the Problem] In order to attain the above-mentioned purpose, the manufacture approach of a three-dimension image processing system according to claim 1 is characterized by pasting up the transparence substrate equipped with the lens which condenses light, and the photo-electric-conversion substrate which was electrically connected to this optoelectric transducer while the optoelectric transducer was formed in the principal plane and with which it embedded and wiring was formed so that the rear face of a transparence substrate and the principal plane of a photo-electric-conversion substrate may counter, and manufacturing a three-dimension image processing system.
[0012] The transparence substrate equipped with the lens which condenses light in invention of claim 1, without using a support substrate etc., In order to paste up the photo-electric-conversion substrate which was electrically connected to this optoelectric transducer and with which it embedded and wiring was formed so that the rear face of a transparence substrate and the principal plane of a photo-electric-conversion substrate may counter while an optoelectric transducer is formed in a principal plane, A transparence substrate can be used as a transparence substrate of image sensors as it is, and the adhesion process to a support substrate, the removal process from a support substrate, and the formation process of a transparence substrate are unnecessary, and can simplify sharply the production process of a three-dimension image processing system. Moreover, since it sticks with a transparence substrate after embedding at a photo-electric-conversion substrate and forming wiring, embedding wiring surrounded by the reliable insulator layer can be formed.
[0013] The manufacture approach of a three-dimension image processing system according to claim 2 In invention of claim 1, grind the rear-face side of said photo-electric-conversion

substrate, and said embedding wiring is exposed. The magnification conversion substrate which was electrically connected to this amplifier and the analog-to-digital converter while the amplifier and the analog-to-digital converter were formed in the principal plane at the rear face of this photo-electric-conversion substrate and with which it embedded and wiring was formed It is characterized by pasting up so that this amplifier and an analog-to-digital converter may be electrically connected to the outcrop of said embedding wiring, and manufacturing a three-dimension image processing system.

[0014] According to invention of claim 2, the three-dimension image processing system which carried out the laminating of the magnification conversion substrate which was electrically connected to the amplifier and the analog-to-digital converter according to the simple and easy process of polish and adhesion, and with which it embedded and wiring was formed to the image-sensors section which consists of a transparence substrate and a photo-electric-conversion substrate can be manufactured.

[0015] The manufacture approach of a three-dimension image processing system according to claim 3 In invention of claim 2, grind the rear-face side of said magnification conversion substrate, and said embedding wiring is exposed. The data storage substrate which was electrically connected to this data storage while data storage was formed in the principal plane at the rear face of this magnification conversion substrate and with which it embedded and wiring was formed It is characterized by pasting up so that this data storage may be electrically connected to the outcrop of said embedding wiring, and manufacturing a three-dimension image processing system.

[0016] According to invention of claim 3, the three-dimension image processing system which carried out the laminating of the data storage substrate which was electrically connected to data storage while the store was formed in the principal plane of the simple and easy process of polish and adhesion, and with which it embedded and wiring was formed to the layered product by which the magnification conversion substrate was formed in the image-sensors section which consists of a transparence substrate and a photo-electric-conversion substrate of polish and adhesion can be manufactured.

[0017] The manufacture approach of a three-dimension image processing system according to claim 4 In invention of claim 2, grind the rear-face side of said data storage substrate, and said embedding wiring is exposed. The data-processing substrate which was electrically connected to this data processor while the data processor was formed in the principal plane at the rear face of this data storage substrate and with which it embedded and wiring was formed It is characterized by pasting up so that this data processor may be electrically connected to the outcrop of said embedding wiring, and manufacturing a three-dimension image processing system.

[0018] According to invention of claim 4, the three-dimension image processing system which carried out the laminating of the data-processing substrate which was electrically connected to this data processor while the data processor was formed in the principal plane of the simple and easy process of polish and adhesion, and with which it embedded and wiring was formed to the layered product by which the magnification conversion substrate and the data storage substrate were formed in the image-sensors section which consists of a transparence substrate and a photo-electric-conversion substrate of polish and adhesion can be manufactured.

[0019] The manufacture approach of a three-dimension image processing system according to claim 5 In invention of claim 4, grind the rear-face side of said data-processing substrate, and said embedding wiring is exposed. This output circuit pastes up the output circuit substrate which was electrically connected to this output circuit while the output circuit was formed in the principal plane and with which it embedded and wiring was formed on the rear face of this data-processing substrate so that it may connect with the outcrop of said embedding wiring electrically. It is characterized by manufacturing a three-dimension image processing system.

[0020] According to invention of claim 5, the three-dimension image processing system which carried out the laminating of the output circuit substrate which was electrically connected to the layered product by which the magnification conversion substrate, the data storage substrate, and the data processor were formed in the image-sensors section which consists of a transparence

substrate and a photo-electric-conversion substrate of polish and adhesion according to it in this output circuit while the output circuit was formed in the principal plane of the simple and easy process of polish and adhesion, and with which it embedded and wiring was formed can be manufactured.

[0021]

[Embodiment of the Invention] Hereafter, the manufacture approach of the three-dimension image processing system of this invention is explained concretely, referring to a drawing. Drawing 1 - drawing 5 are the sectional views showing each process of the manufacture approach of the three-dimension image processing system of this invention.

[0022] First, as shown in drawing 1 , the transparence substrate 10 made from quartz glass with which many micro lenses 12 were formed in the shape of two-dimensional is pasted up on the photo-electric-conversion substrate 20 through the adhesives 14 which consist of polymeric materials, such as an epoxy resin and polyimide resin, so that the principal plane of the photo-electric-conversion substrate 20 and the rear face of the transparence substrate 10 may counter.

[0023] The photo-electric-conversion substrate 20 used above forms a photodiode and an MOS transistor on n mold silicon crystal substrate 16 with which the insulating layer 36 which consists of NI silicon oxide was inserted in the interior. A photodiode forms p mold impurity layer 18 on n mold silicon crystal substrate 16 of the photo-electric-conversion substrate 20, and is formed by forming n mold impurity layer 22 in the field corresponding to the focal location of the micro lens 12 of p mold impurity layer 18 surface. Moreover, the MOS transistor is formed by forming n mold impurity layer 22 used as the source and a drain in parts other than the image pick-up field of p mold impurity layer 18 surface, and forming the gate electrode 26 which consists of polish recon mutually insulated by insulator layer 24A on p mold impurity layer 18 between this n mold impurity layer 22. In addition, the adjoining MOS transistor is separated by the component demarcation membrane 30 which consists of NI silicon oxide.

[0024] Moreover, the trench (deep groove) which penetrates the component demarcation membrane 30 and arrives at the rear face of the photo-electric-conversion substrate 20 is prepared in the photo-electric-conversion substrate 20. In addition, such a trench can be formed by inductive-coupling mold plasma etching etc. An insulator layer 32 is formed in the internal surface of this trench, in the trench, it fills up with an electrical conducting material, and embeds, and wiring 34 is formed. As an electrical conducting material which forms the embedding wiring 34, metals of low resistance, such as low resistance polycrystalline silicon which doped the impurity, for example, and a tungsten, are used.

[0025] It connects with the source electrode 28 which consists of aluminum, and gets down, and n mold impurity layer 22 used as the source of an MOS transistor is connected to the drain electrode 29 with which n mold impurity layer 22 used as a drain was insulated with the source electrode 28 by insulator layer 24B and which consists of aluminum, for example. This drain electrode 29 is embedded, and is connected to wiring 34, and the charge accumulated in the photodiode which consists of an n-type channel 22 and a p mold impurity layer 18 is transmitted to the amplifier later mentioned through this embedding wiring 34 by impressing a predetermined electrical potential difference to the gate electrode 26.

[0026] Next, as shown in drawing 2 , the photo-electric-conversion substrate 20 adhered to the transparence substrate 10 is ground from a rear-face side by chemical mechanical polishing, and is thin-film-ized. In the NI silicon oxide which constitutes the insulating layer 36 inserted in n mold silicon crystal substrate 16, since polish resistance is larger than silicon, polish stops before an insulating layer 36, and the embedding wiring 34 is exposed from an insulating layer 36. Although the transparence substrate 10 plays the role of a support substrate at this time, since the transparence substrate made from quartz glass which unified and formed the micro lens 12 from the beginning is used, it is not necessary to remove later.

[0027] The image-sensors section equipped with the transparence substrate 10 equipped with the lens which condenses light according to the above process, and the photo-electric-conversion substrate 20 is completed.

[0028] Next, as shown in drawing 3 , the magnification conversion substrate 40 which changes

into a digital signal the analog signal amplified while amplifying the signal from the photo-electric-conversion substrate 20 is pasted up on the rear face of the photo-electric-conversion substrate 20. This magnification conversion substrate 40 forms gate 44A insulated by insulator layer 42A, source 46A, and two or more MOSFET50A (two MOSFETs are illustrated with the gestalt of this operation) which consists of drain 48A on silicon substrate 38A by which insulating-layer 36A which consists of NI silicon oxide was inserted in the interior. MOSFET50A which these-adjoins is separated by component demarcation membrane 52A which consists of NI silicon oxide.

[0029] Moreover, the trench which penetrates this component demarcation membrane 52A, and reaches a circuit side from the rear-face side front face of the magnification conversion substrate 40 is prepared in the magnification conversion substrate 40. Insulator layer 54A is formed in the internal surface of this trench, in the trench, it fills up with an electrical conducting material, and embeds, and wiring 56A is formed. As an electrical conducting material which forms embedding wiring 56A, metals of low resistance, such as low resistance polycrystalline silicon which doped the impurity, for example, and a tungsten, are used. Direct continuation of the aluminum wiring 58A is carried out to the edge by the side of the circuit side of this embedding wiring 56A. The integrated circuit which contains an amplifier (amplifier) and an analog-to-digital converter (ADC) by this is constituted. The formed integrated circuit is covered with insulator layer 60A which consists of NI silicon oxide, and flattening of the front face by the side of the integrated circuit of the magnification conversion substrate 40 is carried out. Moreover, aluminum wiring 58A is pulled out from opening prepared in this insulator layer 60A, and it is exposed to the front face of insulator layer 60A.

[0030] The micro bump 62 is formed in the front face by the side of the rear face of the above-mentioned photo-electric-conversion substrate 20 so that the edge of the embedding wiring 34 exposed from the front face of an insulating layer 36 may be contacted. On the other hand, the micro bump 64 is formed also in the front face of insulator layer 60A or front face by the side of the integrated circuit of the magnification conversion substrate 40 so that the edge of exposed aluminum wiring 58A may be contacted. A micro bump can form by the lift off which used the resist mask, and can use the alloy or indium of gold and an indium as a micro bump's ingredient.

[0031] Temporary adhesion of the photo-electric-conversion substrate 20 is piled up and carried out on the magnification conversion substrate 40 so that the micro bump 62 prepared in the front face by the side of the rear face of the photo-electric-conversion substrate 20 and the micro bump 64 prepared in the front face by the side of the integrated-circuit side of the magnification conversion substrate 40 may be connected electrically. In addition, the alignment equipment using the infrared radiation which penetrates a silicon wafer can perform alignment of the photo-electric-conversion substrate 20 and the magnification conversion substrate 40.

[0032] The photo-electric-conversion substrate 20 which carried out temporary adhesion, and the magnification conversion substrate 40 are put into the chamber in which pressurization is possible with the container holding a liquefied epoxy resin, the photo-electric-conversion substrate 20 and the magnification conversion substrate 40 which made the inside of a chamber the vacuum and carried out temporary adhesion are dipped into a liquefied epoxy resin, it returns to ordinary pressure, and an epoxy resin 66 is poured into the clearance between substrates. A substrate is pulled up after that, an epoxy resin 66 is stiffened, and adhesion with the magnification conversion substrate 40 and the photo-electric-conversion substrate 20 is completed.

[0033] Next, as shown in drawing 4 , from a rear-face side, the magnification conversion substrate 40 is ground in uniform thickness by chemical mechanical polishing, and is thin-film-ized. Since polish resistance is larger than silicon, as for the NI silicon oxide which constitutes insulating-layer 36A, embedding wiring 56A in which polish stops before insulating-layer 36A, and is formed to the location deeper than insulating-layer 36A is exposed from insulating-layer 36A.

[0034] Next, as shown in drawing 5 , the data storage substrate 70 equipped with the data storage (register array) which memorizes data temporarily is pasted up on the rear face of the magnification conversion substrate 40 adhered to the photo-electric-conversion substrate 20. The data storage substrate 70 used here on silicon substrate 38B by which insulating-layer 36B

which consists of NI silicon oxide was inserted in the interior like the magnification conversion substrate 40 Gate 44B insulated by insulator layer 42B, source 46B, and two or more MOSFET50B (two MOSFETs are illustrated with the gestalt of this operation) which consists of drain 48B are formed. Adjoining MOSFET50B is separated by component demarcation membrane 52B which consists of NI silicon oxide.

[0035] Moreover, the trench which penetrates this component demarcation membrane 52B, and reaches a circuit side from the rear-face side front face of the data storage substrate 70 is prepared in the data storage substrate 70. Insulator layer 54B is formed in the internal surface of this trench, in the trench, it fills up with an electrical conducting material, and embeds, and wiring 56B is formed. As an electrical conducting material which forms embedding wiring 56B, metals of low resistance, such as low resistance polycrystalline silicon which doped the impurity, for example, and a tungsten, are used. Direct continuation of the aluminum wiring 58B is carried out to the edge by the side of the circuit side of embedding wiring 56B. The integrated circuit which contains data storage by this is constituted. The formed integrated circuit is covered with insulator layer 60B which consists of NI silicon oxide, and flattening of the front face by the side of the integrated circuit of the data storage substrate 70 is carried out. Aluminum wiring 58B is pulled out from opening prepared in this insulator layer 60B, and it is exposed to the front face of insulator layer 60B.

[0036] The micro bump 71 is formed in the front face by the side of the rear face of the above-mentioned magnification conversion substrate 40 so that the edge of embedding wiring 56A exposed from the front face of insulating-layer 36A may be contacted. On the other hand, the micro bump 72 is formed also in the front face of insulator layer 60B or front face by the side of the integrated circuit of the data storage substrate 70 so that the edge of exposed aluminum wiring 58B may be contacted. With and the micro bump 71 prepared in the front face by the side of the rear face of the magnification conversion substrate 40 Temporary adhesion of the magnification conversion substrate 40 is piled up and carried out on the data storage substrate 70 so that the micro bump 72 prepared in the front face by the side of the integrated circuit of the data storage substrate 70 may be connected electrically. The magnification conversion substrate 40 and the data storage substrate 70 are pasted up with an epoxy resin 74 like the case where the photo-electric-conversion substrate 20 and the magnification conversion substrate 40 are pasted up.

[0037] Next, as shown in drawing 6 , the data-processing substrate 80, the output circuit substrate 90, and the output terminal section 100 are formed in the rear face of the data storage substrate 70 in order. The data storage substrate 70 adhered to the magnification conversion substrate 40 is ground from a rear-face side like the formation process of the above-mentioned magnification conversion substrate 40 or the data storage substrate 70, and the data-processing substrate 80 with which the embedding wiring 82 was formed in preparation for the rear face of the data storage substrate 70 in the data processor (processor array) is pasted up so that the integrated circuit in which it was prepared by both substrates may embed and wiring 82 may connect electrically. Furthermore, after grinding this data-processing substrate 80 from a rear-face side, the output circuit substrate 90 with which it embedded at the rear face of the data-processing substrate 80, and wiring 92 was formed is pasted up so that the integrated circuit in which it was prepared by both substrates may embed and wiring 92 may connect electrically. And the micro bump 93 is formed so that the edge of the embedding wiring 92 which ground the output circuit substrate 90 from the rear-face side, embedded from the insulator layer of output circuit substrate 90 rear face, was made to expose the edge of wiring 92, and was exposed may be contacted.

[0038] And finally the output terminal section 100 is formed in the rear face of the output circuit substrate 90. The embedding wiring 104 which the output terminal section 100 penetrated this silicon substrate 102 to the silicon substrate 102, and was exposed to substrate both-sides side is formed. As an electrical conducting material which forms the embedding wiring 104, metals of low resistance, such as copper, a tungsten, and gold, are used, for example. The micro bump 94 is formed in the front face of the input side of this output terminal section 100 so that one edge of the embedding wiring 104 exposed from the front face of the insulating layer of the output

terminal section 100 may be contacted. And the micro bump 93 prepared in the front face by the side of the rear face of the output circuit substrate 90 and the micro bump 94 prepared in the front face of the input side of the output terminal section 100 contact, and both substrates are pasted up so that the integrated circuit prepared in the output circuit substrate 90 may be electrically connected to the output terminal of the output terminal section 100. And the micro bump 106 is formed in the front face of the output side of the above-mentioned output terminal section 100 so that the other-end section of the embedding wiring 104 may be contacted. The micro bump 106 can form from gold, or indiums or those alloys. Moreover, it is good also as a solder bump.

[0039] The three-dimension image processing system shown in drawing 6 which unified the image-sensors section which consists of the transparence substrate 10 and the photo-electric-conversion substrate 20 which were equipped with the lens which condenses light according to the above process, and the processing section (the magnification conversion substrate 40, the data storage substrate 70, the data-processing substrate 80, and output circuit substrate 90) for processing the signal from the image-sensors section can be obtained.

[0040] With the gestalt of this operation, since many micro lenses paste up a photo-electric-conversion substrate on the transparence substrate made from quartz glass formed in the shape of two-dimensional directly, it is not necessary to prepare a support substrate separately, and the attachment-and-detachment process of a support substrate becomes unnecessary. A production process can be simplified sharply by this and a three-dimension image processing system can be manufactured according to a simple and easy process. Moreover, since embedding wiring of each integrated-circuit substrate is formed before lamination, embedding wiring surrounded by the reliable insulator layer can be formed.

[0041] Although the insulating layer which becomes each semi-conductor substrate for forming an integrated circuit from NI silicon oxide used the silicon substrate formed in the interior with the gestalt of the above-mentioned implementation, the silicon substrate which does not contain the insulating layer which consists of NI silicon oxide may be used.

[0042] Although the gestalt of the above-mentioned implementation explained the example which connects electrically the substrate which a micro bump is formed in the both ends of embedding wiring, and micro bumps are contacted, and adjoins, you may make it connect electrically the substrate which forms a micro bump only in one edge of embedding wiring, and adjoins it.

[0043] In the image-sensors section which consists of a transparence substrate and a photo-electric-conversion substrate equipped with the condenser lens with the gestalt of the above-mentioned implementation Although the example which forms each processing section of the magnification conversion substrate for processing the signal from the image-sensors section, a data storage substrate, a data-processing substrate, and an output circuit substrate by repeating polish and lamination was explained After grinding and embedding the photo-electric-conversion substrate which constitutes the image-sensors section from a rear-face side and exposing wiring, a photo-electric-conversion substrate is also electrically connectable with a magnification conversion substrate with wiring.

[0044] Moreover, after grinding and embedding a magnification conversion substrate from a rear-face side and exposing wiring, a magnification conversion substrate is also electrically connectable [a magnification conversion substrate is formed in the image-sensors section by polish and lamination like the gestalt of the above-mentioned implementation, and] with a data storage substrate with wiring. Moreover, after grinding and embedding a data storage substrate from a rear-face side and exposing wiring, a data storage substrate is also electrically connectable [a magnification conversion substrate and a data storage substrate are formed in the image-sensors section by polish and lamination like the gestalt of the above-mentioned implementation, and] with a data-processing substrate with wiring. Moreover, after grinding and embedding a data-processing substrate from a rear-face side and exposing wiring, a data-processing substrate is also electrically connectable [a magnification conversion substrate, a data storage substrate, and a data-processing substrate are formed in the image-sensors section by polish and lamination like the gestalt of the above-mentioned implementation, and] with an output circuit substrate with wiring.

[0045] In addition, a wafer scale or a chip scale is sufficient as the silicon substrate used in the gestalt of the above-mentioned implementation.
[0046]
[Effect of the Invention] The manufacture approach of the three-dimension image processing system of this invention does so the effectiveness that the attachment-and-detachment process of a support substrate can be unnecessary, can simplify a production process sharply, and can manufacture a three-dimension image processing system according to a simple and easy process. Moreover, the manufacture approach of the three-dimension image processing system of this invention does so the effectiveness surrounded by the reliable insulator layer that it can embed and wiring can be formed.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the outline sectional view showing the production process of the three-dimension image formation equipment of the gestalt of this operation.
[Drawing 2] It is the outline sectional view showing the production process of the three-dimension image formation equipment of the gestalt of this operation.
[Drawing 3] It is the outline sectional view showing the production process of the three-dimension image formation equipment of the gestalt of this operation.
[Drawing 4] It is the outline sectional view showing the production process of the three-dimension image formation equipment of the gestalt of this operation.
[Drawing 5] It is the outline sectional view showing the production process of the three-dimension image formation equipment of the gestalt of this operation.
[Drawing 6] It is the outline sectional view showing the structure of the three-dimension image formation equipment of the gestalt of this operation.
[Description of Notations]
10 Transparence Substrate
12 Micro Lens
16 N Mold Silicon Crystal Substrate
18 P Mold Impurity Layer
20 Photo-Electric-Conversion Substrate
22 N Mold Impurity Layer
26 Gate Electrode
28 Electrode
34 Embedding Wiring
40 Magnification Conversion Substrate
70 Data Storage Substrate
80 Data-Processing Substrate
90 Output Circuit Substrate
100 Output Terminal Section

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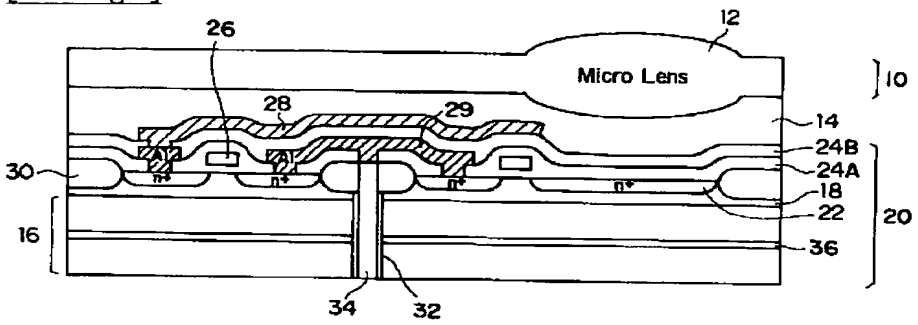
DRAWINGS

[Drawing 1]



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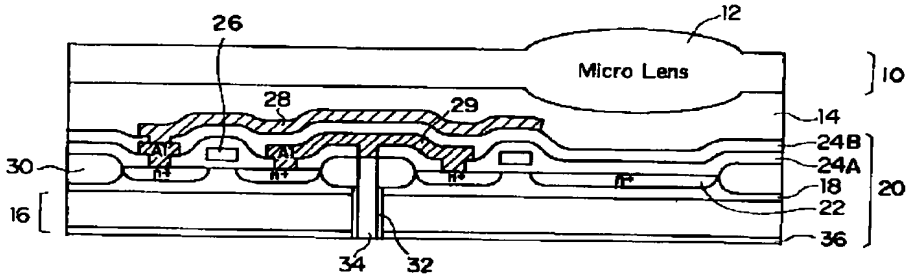

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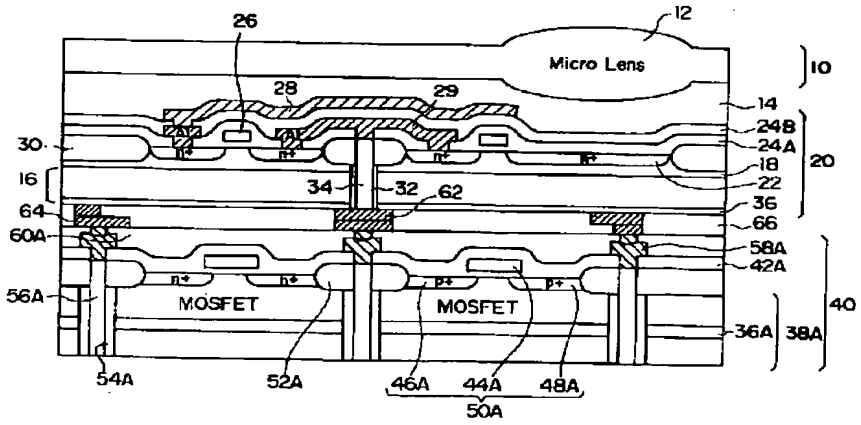

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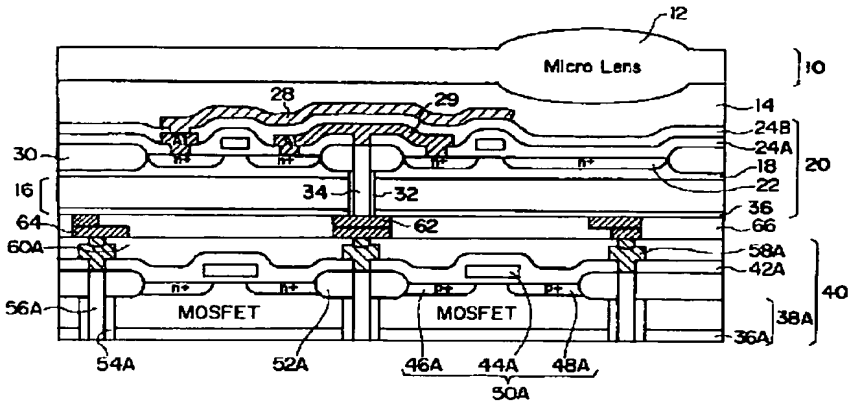

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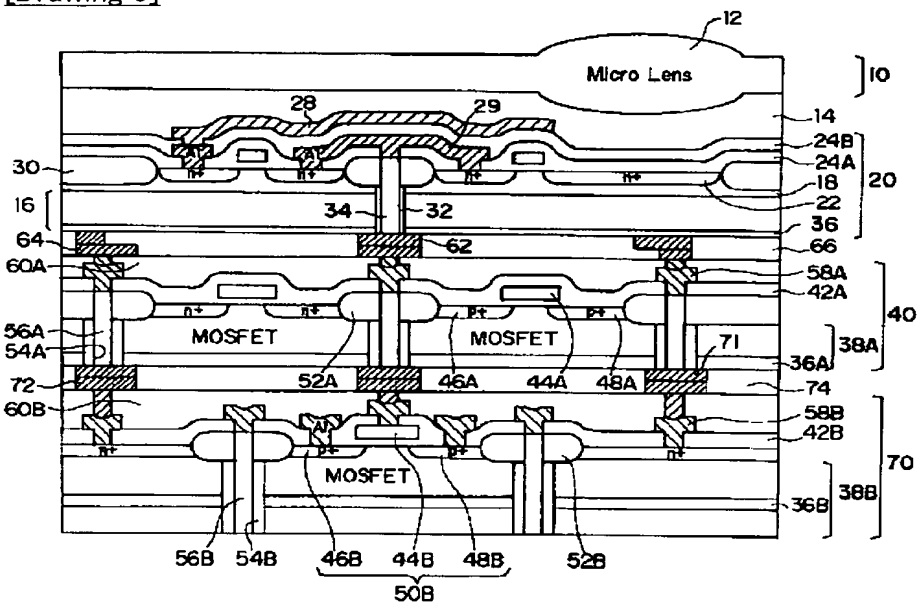

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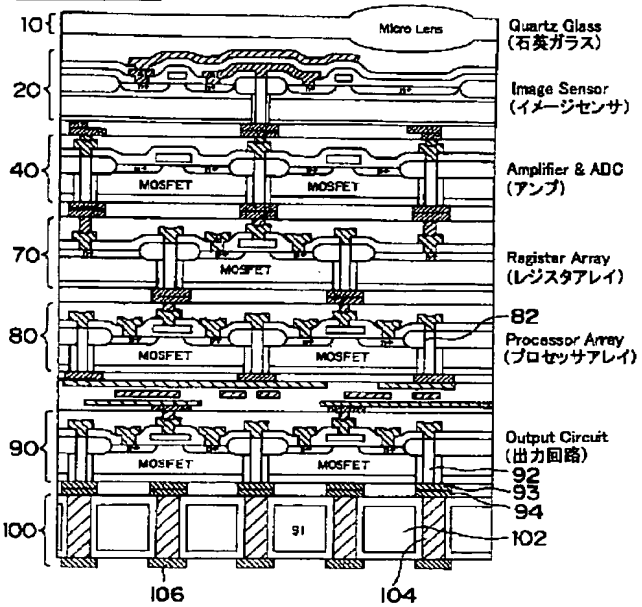

[Translation done.]

(19)日本国特許庁（ＪＰ）　(12)公開特許公報（Ａ）　(11)特許出願公開番号
特開2001－339057
（P2001－339057A）
(43)公開日　平成13年12月７日(2001.12.7)

(51)Int.Cl.⁷	識別記号	FI		テーマコード（参考）
H01L 27/146		G06T 1/00	420A	4M118
G06T 1/00	420	H01L 27/00	301B	5B047
H01L 21/3205		H04N 5/335	U	5C024
21/768		H01L 27/14	F	5F033
27/00	301	21/88	J	5F048

審査請求　未請求　請求項の数５　ＯＬ　（全 9 頁）　最終頁に続く

(21)出願番号　特願2000－160330(P2000－160330)

(22)出願日　平成12年５月30日(2000.5.30)

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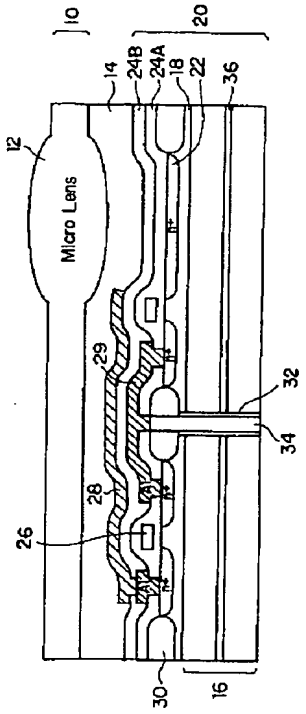
最終頁に続く

(54)【発明の名称】　３次元画像処理装置の製造方法

(57)【要約】
【課題】支持基板の着脱工程が不要で製造工程を大幅に簡略化することができ、簡素かつ容易な工程により３次元画像処理装置を製造することができる３次元画像処理装置の製造方法を提供する。また、信頼性の高い絶縁膜で囲まれた埋め込み配線を形成することができる３次元画像処理装置の製造方法を提供する。
【解決手段】内部に二酸化ケイ素からなる絶縁層３６が挿入されたｎ型シリコン結晶基板１６上に、フォトダイオードとＭＯＳトランジスタとが形成された光電変換基板２０に、多数のマイクロレンズ１２が２次元状に形成された石英ガラス製の透明基板１０を、光電変換基板２０の主面と透明基板１０の裏面とが対向するように、エポキシ樹脂やポリイミド樹脂等の高分子材料からなる接着剤１４を介して接着する。



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【特許請求の範囲】

【請求項１】光を集光するレンズを備えた透明基板と、主面に光電変換素子が形成されると共に該光電変換素子に電気的に接続された埋め込み配線が形成された光電変換基板とを、透明基板の裏面と光電変換基板の主面とが対向するように接着して、３次元画像処理装置を製造する３次元画像処理装置の製造方法。

【請求項２】前記光電変換基板の裏面側を研磨して前記埋め込み配線を露出させ、

該光電変換基板の裏面に、主面に増幅器及びアナログ／デジタル変換器が形成されると共に該増幅器及びアナログ／デジタル変換器に電気的に接続された埋め込み配線が形成された増幅変換基板を、該増幅器及びアナログ／デジタル変換器が前記埋め込み配線の露出部に電気的に接続されるように接着して、３次元画像処理装置を製造する請求項１に記載の３次元画像処理装置の製造方法。

【請求項３】前記増幅変換基板の裏面側を研磨して前記埋め込み配線を露出させ、

該増幅変換基板の裏面に、主面にデータ記憶装置が形成されると共に該データ記憶装置に電気的に接続された埋め込み配線が形成されたデータ記憶基板を、該データ記憶装置が前記埋め込み配線の露出部に電気的に接続されるように接着して、３次元画像処理装置を製造する請求項２に記載の３次元画像処理装置の製造方法。

【請求項４】前記データ記憶基板の裏面側を研磨して前記埋め込み配線を露出させ、

該データ記憶基板の裏面に、主面にデータ処理装置が形成されると共に該データ処理装置に電気的に接続された埋め込み配線が形成されたデータ処理基板を、該データ処理装置が前記埋め込み配線の露出部に電気的に接続されるように接着して、３次元画像処理装置を製造する請求項３に記載の３次元画像処理装置の製造方法。

【請求項５】前記データ処理基板の裏面側を研磨して前記埋め込み配線を露出させ、

該データ処理基板の裏面に、主面に出力回路が形成されると共に該出力回路に電気的に接続された埋め込み配線が形成された出力回路基板を、該出力回路が前記埋め込み配線の露出部に電気的に接続されるように接着して、３次元画像処理装置を製造する請求項４に記載の３次元画像処理装置の製造方法。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、３次元画像処理装置の製造方法に関する。

【０００２】

【従来の技術】近年、半導体集積回路装置の高集積化・高密度化等の目的から、複数の回路機能ブロックを立体的に集積した３次元半導体集積回路装置の開発が進められている。特に、イメージセンサとその信号を処理するための信号処理回路を一体化した３次元画像処理装置

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（インテリジェントイメージプロセッサ）は、光センサから得られる画像データを並列に高速処理し、高画質画像をリアルタイムで得ることが可能になることから、多くの期待が寄せられている。

【０００３】これら３次元半導体集積回路装置は、当初はレーザ再結晶化等によるＳＯＩ（Silicon On Insulator）技術を利用してＳＯＩ基板形成とＳＯＩ基板への半導体装置の形成を繰り返すモノリシック法によりその製造が検討されてきたが、ＳＯＩを多層に積層するには、結晶性の確保が難しい、製造時間が長い等の問題があった。

【０００４】このため、半導体装置または半導体集積回路装置が予め作製された単結晶半導体基板同士を貼り合わせる貼り合わせ技術による３次元半導体集積回路装置の製造方法が種々検討されている。

【０００５】月刊セミコンダクターワールド（林善宏等、１９９０年９月号ｐ５８～６４）には、貼り合わせ技術の一種として、研磨により薄膜化した半導体基板を貼り合わせるＣＵＢＩＣ技術が提案されている。ＣＵＢＩＣ技術では、まずシリコン基板上に半導体素子が形成された第１の半導体基板を支持基板に接着した後、余分なシリコン基板をポリッシングして薄膜化する。次に、埋め込み配線、裏面配線、バンプ／プールからなるコンタクト部材等のデバイスの縦方向の接続に必要な配線を形成し、第１の半導体基板とシリコン基板上に半導体素子の形成された第２の半導体基板とを貼り合わせる。そして最後に支持基板を取り外して多層構造の半導体装置が完成する。

【０００６】また、特開平６－２６０５９４号公報には、貼り合わせ技術による３次元半導体集積回路装置の製造方法が開示されている。この方法は、シリコン基板上に半導体素子が形成された第１の半導体基板を支持基板に接着した後、余分なシリコン基板をポリッシングして薄膜化する点はＣＵＢＩＣ技術と共通しているが、第１の半導体基板に予め埋め込み配線を形成するための深溝が設けられている点、及び第１の半導体基板とシリコン基板上に半導体素子の形成された第２の半導体基板とを貼り合わせ、貼り合わせ後に支持基板を取り除き埋め込み配線を形成する点で、ＣＵＢＩＣ技術とは異なっている。

【０００７】

【発明が解決しようとする課題】しかしながら、いずれの製造方法も、第１の半導体基板を支持基板に貼り合わせ、研磨した後に支持基板から第１の半導体基板を剥離する工程を含んでおり、製造工程が煩雑であるという問題があった。特に、３次元画像処理装置を製造する場合には、支持基板を取り除いた後にその表面にイメージセンサを構成するマイクロレンズを備えた透明基板を設ける必要があるため、なおさら製造工程が煩雑になる。

【０００８】また、ＣＵＢＩＣ技術では、余分なシリコ

ン基板をポリッシングして薄膜化した後に支持基板を取り除くため、支持基板を取り除く際に半導体基板上に形成された集積回路が破損するという問題があった。

【０００９】また、特開平６－２６０５９４号公報に記載された方法では、埋め込み配線を形成するための深溝が予め設けられた第１の半導体基板を支持基板に接着するため、深溝に入り込んだ接着剤の除去が困難であるという問題や、第１の半導体基板と第２の半導体基板とを接着した後に深溝の側壁を酸化して絶縁膜を形成するため、接着剤の耐熱温度以上に酸化温度を上げることができず、信頼性のある絶縁膜を形成することができないという問題があった。

【００１０】本発明は上記従来技術の問題点に鑑みなされたものであり、本発明の目的は、支持基板の着脱工程が不要で製造工程を大幅に簡略化することができ、簡素かつ容易な工程により３次元画像処理装置を製造することができる３次元画像処理装置の製造方法を提供することにある。また、本発明の他の目的は、信頼性の高い絶縁膜で囲まれた埋め込み配線を形成することができる３次元画像処理装置の製造方法を提供することにある。

【００１１】

【課題を解決するための手段】上記目的を達成するために、請求項１に記載の３次元画像処理装置の製造方法は、光を集光するレンズを備えた透明基板と、主面に光電変換素子が形成されると共に該光電変換素子に電気的に接続された埋め込み配線が形成された光電変換基板とを、透明基板の裏面と光電変換基板の主面とが対向するように接着して、３次元画像処理装置を製造することを特徴とする。

【００１２】請求項１の発明では、支持基板等を用いることなく、光を集光するレンズを備えた透明基板と、主面に光電変換素子が形成されると共に該光電変換素子に電気的に接続された埋め込み配線が形成された光電変換基板とを、透明基板の裏面と光電変換基板の主面とが対向するように接着するため、透明基板をそのままイメージセンサの透明基板として使用することができ、支持基板への接着工程、支持基板からの除去工程、及び透明基板の形成工程が不要であり、３次元画像処理装置の製造工程を大幅に簡略化することができる。また、光電変換基板に埋め込み配線を形成した後に透明基板と貼り合わせるため、信頼性の高い絶縁膜で囲まれた埋め込み配線を形成することができる。

【００１３】請求項２に記載の３次元画像処理装置の製造方法は、請求項１の発明において、前記光電変換基板の裏面側を研磨して前記埋め込み配線を露出させ、該光電変換基板の裏面に、主面に増幅器及びアナログ／デジタル変換器が形成されると共に該増幅器及びアナログ／デジタル変換器に電気的に接続された埋め込み配線が形成された増幅変換基板を、該増幅器及びアナログ／デジタル変換器が前記埋め込み配線の露出部に電気的に接続されるように接着して、３次元画像処理装置を製造することを特徴とする。

【００１４】請求項２の発明によれば、透明基板及び光電変換基板からなるイメージセンサ部に、研磨及び接着という簡素かつ容易な工程により、増幅器及びアナログ／デジタル変換器に電気的に接続された埋め込み配線が形成された増幅変換基板を積層した３次元画像処理装置を製造することができる。

【００１５】請求項３に記載の３次元画像処理装置の製造方法は、請求項２の発明において、前記増幅変換基板の裏面側を研磨して前記埋め込み配線を露出させ、該増幅変換基板の裏面に、主面にデータ記憶装置が形成されると共に該データ記憶装置に電気的に接続された埋め込み配線が形成されたデータ記憶基板を、該データ記憶装置が前記埋め込み配線の露出部に電気的に接続されるように接着して、３次元画像処理装置を製造することを特徴とする。

【００１６】請求項３の発明によれば、透明基板及び光電変換基板からなるイメージセンサ部に研磨と接着とにより増幅変換基板が形成された積層体に、研磨及び接着という簡素かつ容易な工程により、主面に記憶装置が形成されると共にデータ記憶装置に電気的に接続された埋め込み配線が形成されたデータ記憶基板を積層した３次元画像処理装置を製造することができる。

【００１７】請求項４に記載の３次元画像処理装置の製造方法は、請求項２の発明において、前記データ記憶基板の裏面側を研磨して前記埋め込み配線を露出させ、該データ記憶基板の裏面に、主面にデータ処理装置が形成されると共に該データ処理装置に電気的に接続された埋め込み配線が形成されたデータ処理基板を、該データ処理装置が前記埋め込み配線の露出部に電気的に接続されるように接着して、３次元画像処理装置を製造することを特徴とする。

【００１８】請求項４の発明によれば、透明基板及び光電変換基板からなるイメージセンサ部に研磨と接着とにより増幅変換基板及びデータ記憶基板が形成された積層体に、研磨及び接着という簡素かつ容易な工程により、主面にデータ処理装置が形成されると共に該データ処理装置に電気的に接続された埋め込み配線が形成されたデータ処理基板を積層した３次元画像処理装置を製造することができる。

【００１９】請求項５に記載の３次元画像処理装置の製造方法は、請求項４の発明において、前記データ処理基板の裏面側を研磨して前記埋め込み配線を露出させ、該データ処理基板の裏面に、主面に出力回路が形成されると共に該出力回路に電気的に接続された埋め込み配線が形成された出力回路基板を、該出力回路が前記埋め込み配線の露出部に電気的に接続されるように接着して、３次元画像処理装置を製造することを特徴とする。

【００２０】請求項５の発明によれば、透明基板及び光

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電変換基板からなるイメージセンサ部に研磨と接着とにより増幅変換基板、データ記憶基板、及びデータ処理装置が形成された積層体に、研磨及び接着という簡素かつ容易な工程により、主面に出力回路が形成されると共に該出力回路に電気的に接続された埋め込み配線が形成された出力回路基板を積層した３次元画像処理装置を製造することができる。

【００２１】

【発明の実施の形態】以下、本発明の３次元画像処理装置の製造方法を、図面を参照しつつ具体的に説明する。図１～図５は、本発明の３次元画像処理装置の製造方法の各工程を示す断面図である。

【００２２】まず、図１に示すように、光電変換基板２０に、多数のマイクロレンズ１２が２次元状に形成された石英ガラス製の透明基板１０を、光電変換基板２０の主面と透明基板１０の裏面とが対向するように、エポキシ樹脂やポリイミド樹脂等の高分子材料からなる接着剤１４を介して接着する。

【００２３】上記で用いる光電変換基板２０は、内部に二酸化ケイ素からなる絶縁層３６が挿入されたｎ型シリコン結晶基板１６上に、フォトダイオードとＭＯＳトランジスタとを形成したものである。フォトダイオードは、光電変換基板２０のｎ型シリコン結晶基板１６上にｐ型不純物層１８を形成し、ｐ型不純物層１８表層のマイクロレンズ１２の焦点位置に対応する領域にｎ型不純物層２２を設けることにより形成されている。また、ＭＯＳトランジスタは、ｐ型不純物層１８表層の撮像領域以外の部分にソース及びドレインとなるｎ型不純物層２２を設け、このｎ型不純物層２２間のｐ型不純物層１８上に絶縁膜２４Ａにより相互に絶縁されたポリシリコンからなるゲート電極２６を設けることにより形成されている。なお、隣接するＭＯＳトランジスタは二酸化ケイ素からなる素子分離膜３０で分離されている。

【００２４】また、光電変換基板２０には、素子分離膜３０を貫通し光電変換基板２０の裏面に達するトレンチ（深溝）が設けられている。なお、このようなトレンチは誘導結合型プラズマエッチング等により形成することができる。このトレンチの内表面に絶縁膜３２が形成され、トレンチ内に導電材料が充填されて埋め込み配線３４が形成されている。埋め込み配線３４を形成する導電材料としては、例えば不純物をドープした低抵抗多結晶シリコンやタングステン等の低抵抗の金属が使用される。

【００２５】ＭＯＳトランジスタのソースとなるｎ型不純物層２２は、例えばアルミニウムからなるソース電極２８に接続されおり、ドレインとなるｎ型不純物層２２は、絶縁膜２４Ｂによりソース電極２８と絶縁された例えばアルミニウムからなるドレイン電極２９に接続されている。このドレイン電極２９は埋め込み配線３４に接続されており、ゲート電極２６に所定電圧を印加することによりｎ型チャネル２２及びｐ型不純物層１８からなるフォトダイオードに蓄積された電荷はこの埋め込み配線３４を介して後述する増幅器へと転送される。

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【００２６】次に、図２に示すように、透明基板１０に接着された光電変換基板２０を、化学的機械研磨により裏面側から研磨して薄膜化する。ｎ型シリコン結晶基板１６に挿入された絶縁層３６を構成する二酸化ケイ素はシリコンよりも研磨耐性が大きいため、研磨は絶縁層３６の手前で止まり、埋め込み配線３４が絶縁層３６から露出される。このとき透明基板１０が支持基板の役割を果たすが、当初からマイクロレンズ１２を一体化して形成した石英ガラス製の透明基板を用いているので後で取り外す必要はない。

【００２７】以上の工程により、光を集光するレンズを備えた透明基板１０、及び光電変換基板２０を備えたイメージセンサ部が完成する。

【００２８】次に、図３に示すように、光電変換基板２０の裏面に、光電変換基板２０からの信号を増幅すると共に増幅されたアナログ信号をデジタル信号に変換する増幅変換基板４０を接着する。この増幅変換基板４０は、内部に二酸化ケイ素からなる絶縁層３６Ａが挿入されたシリコン基板３８Ａ上に、絶縁膜４２Ａにより絶縁されたゲート４４Ａ、ソース４６Ａ、及びドレイン４８Ａからなる複数のＭＯＳＦＥＴ５０Ａ（本実施の形態では２つのＭＯＳＦＥＴを図示する）を形成したものである。これら隣接するＭＯＳＦＥＴ５０Ａは、二酸化ケイ素からなる素子分離膜５２Ａにより分離されている。

【００２９】また、増幅変換基板４０には、この素子分離膜５２Ａを貫通し増幅変換基板４０の裏面側表面から回路面に達するトレンチが設けられている。このトレンチの内表面に絶縁膜５４Ａが形成され、トレンチ内に導電材料が充填されて埋め込み配線５６Ａが形成されている。埋め込み配線５６Ａを形成する導電材料としては、例えば不純物をドープした低抵抗多結晶シリコンやタングステン等の低抵抗の金属が使用される。この埋め込み配線５６Ａの回路面側の端部にはアルミニウム配線５８Ａが直接接続されている。これにより増幅器（アンプ）及びアナログ／デジタル変換器（ＡＤＣ）を含む集積回路が構成されている。形成された集積回路は二酸化ケイ素からなる絶縁膜６０Ａにより被覆され、増幅変換基板４０の集積回路側の表面が平坦化されている。また、この絶縁膜６０Ａに設けられた開口からアルミニウム配線５８Ａが引き出され、絶縁膜６０Ａの表面に露出されている。

【００３０】上記光電変換基板２０の裏面側の表面に、絶縁層３６の表面から露出した埋め込み配線３４の端部に接触するようにマイクロバンプ６２を形成する。一方、増幅変換基板４０の集積回路側の表面にも、絶縁膜６０Ａの表面に露出したアルミニウム配線５８Ａの端部に接触するようにマイクロバンプ６４を形成する。マイ

クロバンプは、レジストマスクを用いたリフトオフ等により形成することができ、マイクロバンプの材料としては例えば金とインジウムとの合金またはインジウムを用いることができる。

【００３１】光電変換基板２０の裏面側の表面に設けられたマイクロバンプ６２と、増幅変換基板４０の集積回路面側の表面に設けられたマイクロバンプ６４とが電気的に接続されるように、増幅変換基板４０上に光電変換基板２０を重ね合わせて仮接着する。なお、光電変換基板２０と増幅変換基板４０との位置合わせは、例えばシリコンウエハを透過する赤外線を用いた位置合わせ装置により行うことができる。

【００３２】仮接着した光電変換基板２０と増幅変換基板４０とを、液状のエポキシ樹脂を保持した容器と共に気圧調整が可能なチャンバーに入れてチャンバー内を真空にし、仮接着した光電変換基板２０と増幅変換基板４０とを液状のエポキシ樹脂にディップして常圧に戻し基板間の隙間にエポキシ樹脂６６を注入する。その後基板を引き上げエポキシ樹脂６６を硬化させて、増幅変換基板４０と光電変換基板２０との接着が完了する。

【００３３】次に、図４に示すように、増幅変換基板４０を裏面側から化学的機械研磨により均一な厚さに研磨して薄膜化する。絶縁層３６Ａを構成するニ酸化ケイ素はシリコンよりも研磨耐性が大きいため、研磨は絶縁層３６Ａの手前で止まり、絶縁層３６Ａよりも深い位置まで形成されている埋め込み配線５６Ａが絶縁層３６Ａから露出される。

【００３４】次に、図５に示すように、光電変換基板２０に接着された増幅変換基板４０の裏面に、一時的にデータを記憶するデータ記憶装置（レジスタアレイ）を備えたデータ記憶基板７０を接着する。ここで用いるデータ記憶基板７０は、増幅変換基板４０と同様に、内部にニ酸化ケイ素からなる絶縁層３６Ｂが挿入されたシリコン基板３８Ｂ上に、絶縁膜４２Ｂにより絶縁されたゲート４４Ｂ、ソース４６Ｂ、及びドレイン４８Ｂからなる複数のＭＯＳＦＥＴ５０Ｂ（本実施の形態では２つのＭＯＳＦＥＴを図示する）を形成したものであり、隣接するＭＯＳＦＥＴ５０Ｂは、ニ酸化ケイ素からなる素子分離膜５２Ｂにより分離されている。

【００３５】また、データ記憶基板７０には、この素子分離膜５２Ｂを貫通しデータ記憶基板７０の裏面側表面から回路面に達するトレンチが設けられている。このトレンチの内表面に絶縁膜５４Ｂが形成され、トレンチ内に導電材料が充填されて埋め込み配線５６Ｂが形成されている。埋め込み配線５６Ｂを形成する導電材料としては、例えば不純物をドープした低抵抗多結晶シリコンやタングステン等の低抵抗の金属が使用される。埋め込み配線５６Ｂの回路面側の端部にはアルミニウム配線５８Ｂが直接接続されている。これによりデータ記憶装置を含む集積回路が構成されている。形成された集積回路は、ニ酸化ケイ素からなる絶縁膜６０Ｂにより被覆され、データ記憶基板７０の集積回路側の表面が平坦化されている。この絶縁膜６０Ｂに設けられた開口からアルミニウム配線５８Ｂが引き出されて、絶縁膜６０Ｂの表面に露出されている。

【００３６】上記増幅変換基板４０の裏面側の表面に、絶縁層３６Ａの表面から露出した埋め込み配線５６Ａの端部に接触するようにマイクロバンプ７１を形成する。一方、データ記憶基板７０の集積回路側の表面にも、絶縁膜６０Ｂの表面に露出したアルミニウム配線５８Ｂの端部に接触するようにマイクロバンプ７２を形成する。そして増幅変換基板４０の裏面側の表面に設けられたマイクロバンプ７１と、データ記憶基板７０の集積回路側の表面に設けられたマイクロバンプ７２とが電気的に接続されるようにデータ記憶基板７０上に増幅変換基板４０を重ね合わせて仮接着し、光電変換基板２０及び増幅変換基板４０を接着する場合と同様にして、増幅変換基板４０とデータ記憶基板７０とをエポキシ樹脂７４により接着する。

【００３７】次に、図６に示すように、データ記憶基板７０の裏面に、データ処理基板８０、出力回路基板９０、及び出力端子部１００を順に形成する。上記増幅変換基板４０やデータ記憶基板７０の形成工程と同様にして、増幅変換基板４０に接着されたデータ記憶基板７０を裏面側から研磨し、データ記憶基板７０の裏面に、データ処理装置（プロセッサアレイ）を備え埋め込み配線８２の形成されたデータ処理基板８０を、両基板に設けられた集積回路が埋め込み配線８２により電気的に接続されるように接着する。さらに、このデータ処理基板８０を裏面側から研磨した後に、データ処理基板８０の裏面に埋め込み配線９２の形成された出力回路基板９０を、両基板に設けられた集積回路が埋め込み配線９２により電気的に接続されるように接着する。そして出力回路基板９０を裏面側から研磨して、出力回路基板９０裏面の絶縁膜から埋め込み配線９２の端部を露出させ、露出した埋め込み配線９２の端部に接触するようにマイクロバンプ９３を形成する。

【００３８】そして最後に出力回路基板９０の裏面に出力端子部１００を形成する。出力端子部１００はシリコン基板１０２にこのシリコン基板１０２を貫通し基板両面側に露出した埋め込み配線１０４が形成されたものである。埋め込み配線１０４を形成する導電材料としては、例えば銅、タングステン、金等の低抵抗の金属が使用される。この出力端子部１００の入力側の表面に、出力端子部１００の絶縁層の表面から露出した埋め込み配線１０４の一方の端部に接触するようにマイクロバンプ９４を形成する。そして出力回路基板９０の裏面側の表面に設けられたマイクロバンプ９３と出力端子部１００の入力側の表面に設けられたマイクロバンプ９４とが接触し、出力回路基板９０に設けられた集積回路が出力端

子部１００の出力端子に電気的に接続されるように両基板を接着する。そして上記出力端子部１００の出力側の表面には、埋め込み配線１０４の他方の端部に接触するようにマイクロバンプ１０６を形成する。マイクロバンプ１０６は、例えば金やインジウムまたはそれらの合金から形成することができる。また、はんだバンプとしてもよい。

【００３９】以上の工程により、光を集光するレンズを備えた透明基板１０及び光電変換基板２０からなるイメージセンサ部と、そのイメージセンサ部からの信号を処理するための処理部（増幅変換基板４０、データ記憶基板７０、データ処理基板８０及び出力回路基板９０）とを一体化した図６に示す３次元画像処理装置を得ることができる。

【００４０】本実施の形態では、多数のマイクロレンズが２次元状に形成された石英ガラス製の透明基板に光電変換基板を直接接着するので、支持基板を別途用意する必要がなく支持基板の着脱工程が不要となる。これにより製造工程を大幅に簡略化することができ、簡素かつ容易な工程により３次元画像処理装置を製造することができる。また、各集積回路基板の埋め込み配線は貼り合わせ前に形成されるので、信頼性の高い絶縁膜で囲まれた埋め込み配線を形成することができる。

【００４１】上記実施の形態では、集積回路を形成するための各半導体基板に二酸化ケイ素からなる絶縁層が内部に形成されたシリコン基板を使用したが、二酸化ケイ素からなる絶縁層を含まないシリコン基板を使用してもよい。

【００４２】上記実施の形態では、埋め込み配線の両端部にマイクロバンプを形成し、マイクロバンプ同士を接触させて隣接する基板を電気的に接続する例について説明したが、埋め込み配線の一方の端部にのみマイクロバンプを形成して隣接する基板を電気的に接続するようにしても良い。

【００４３】上記実施の形態では、集光レンズを備えた透明基板及び光電変換基板からなるイメージセンサ部に、そのイメージセンサ部からの信号を処理するための増幅変換基板、データ記憶基板、データ処理基板、及び出力回路基板の各処理部を研磨及び貼合せを繰り返すことにより形成する例について説明したが、イメージセンサ部を構成する光電変換基板を裏面側から研磨して埋め込み配線を露出させた後、配線により光電変換基板を増幅変換基板と電気的に接続することもできる。

【００４４】また、上記実施の形態と同様にしてイメージセンサ部に研磨及び貼合せにより増幅変換基板を形成し、増幅変換基板を裏面側から研磨して埋め込み配線を露出させた後、配線により増幅変換基板をデータ記憶基板と電気的に接続することもできる。また、上記実施の形態と同様にしてイメージセンサ部に研磨及び貼合せにより増幅変換基板及びデータ記憶基板を形成し、データ記憶基板を裏面側から研磨して埋め込み配線を露出させた後、配線によりデータ記憶基板をデータ処理基板と電気的に接続することもできる。また、上記実施の形態と同様にしてイメージセンサ部に研磨及び貼合せにより増幅変換基板、データ記憶基板、及びデータ処理基板を形成し、データ処理基板を裏面側から研磨して埋め込み配線を露出させた後、配線によりデータ処理基板を出力回路基板と電気的に接続することもできる。

【００４５】なお、上記実施の形態において使用するシリコン基板は、ウエハスケールでもチップスケールでもよい。

【００４６】

【発明の効果】本発明の３次元画像処理装置の製造方法は、支持基板の着脱工程が不要で、製造工程を大幅に簡略化することができ、簡素かつ容易な工程により３次元画像処理装置を製造することができる、という効果を奏する。また、本発明の３次元画像処理装置の製造方法は、信頼性の高い絶縁膜で囲まれた埋め込み配線を形成することができる、という効果を奏する。

【図面の簡単な説明】

【図１】本実施の形態の３次元画像形成装置の製造工程を示す概略断面図である。

【図２】本実施の形態の３次元画像形成装置の製造工程を示す概略断面図である。

【図３】本実施の形態の３次元画像形成装置の製造工程を示す概略断面図である。

【図４】本実施の形態の３次元画像形成装置の製造工程を示す概略断面図である。

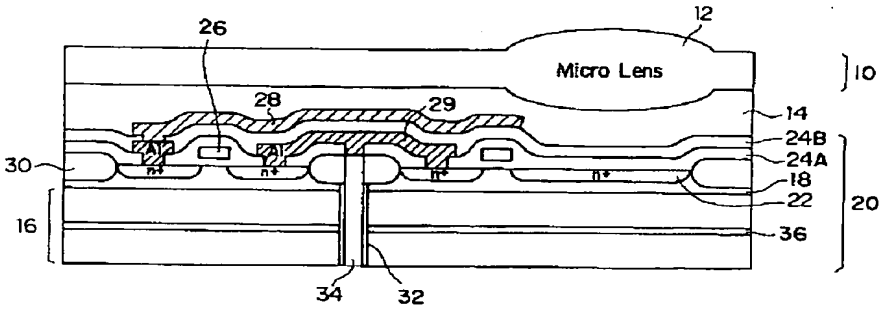
【図５】本実施の形態の３次元画像形成装置の製造工程を示す概略断面図である。

【図６】本実施の形態の３次元画像形成装置の構造を示す概略断面図である。

【符号の説明】

１０　透明基板
１２　マイクロレンズ
１６　ｎ型シリコン結晶基板
１８　ｐ型不純物層
２０　光電変換基板
２２　ｎ型不純物層
２６　ゲート電極
２８　電極
３４　埋め込み配線
４０　増幅変換基板
７０　データ記憶基板
８０　データ処理基板
９０　出力回路基板
１００　出力端子部

【図１】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24A
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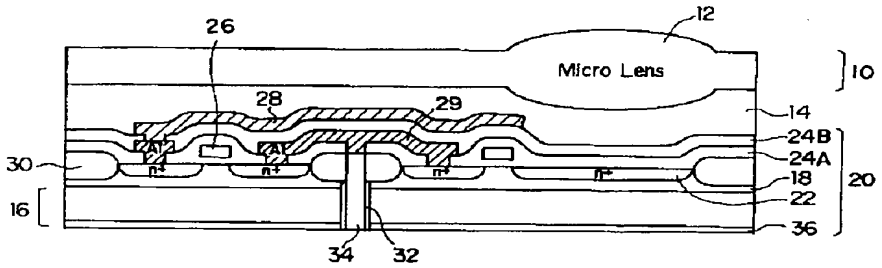
34
32

【図２】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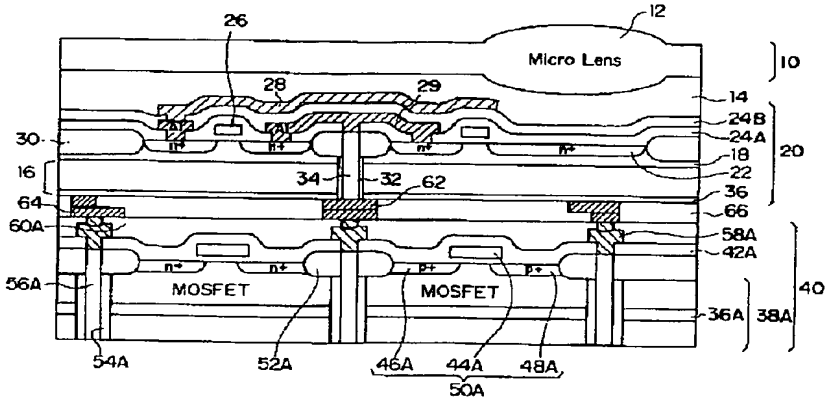
【図３】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66
60A
58A
42A
MOSFET
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36A
38A
54A
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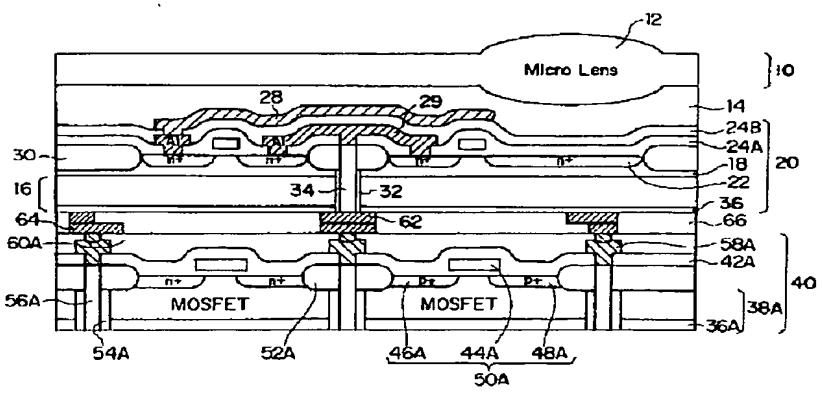
46A
44A
48A
50A

【図４】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66
60A
58A
42A
40
56A
MOSFET
MOSFET
38A
36A
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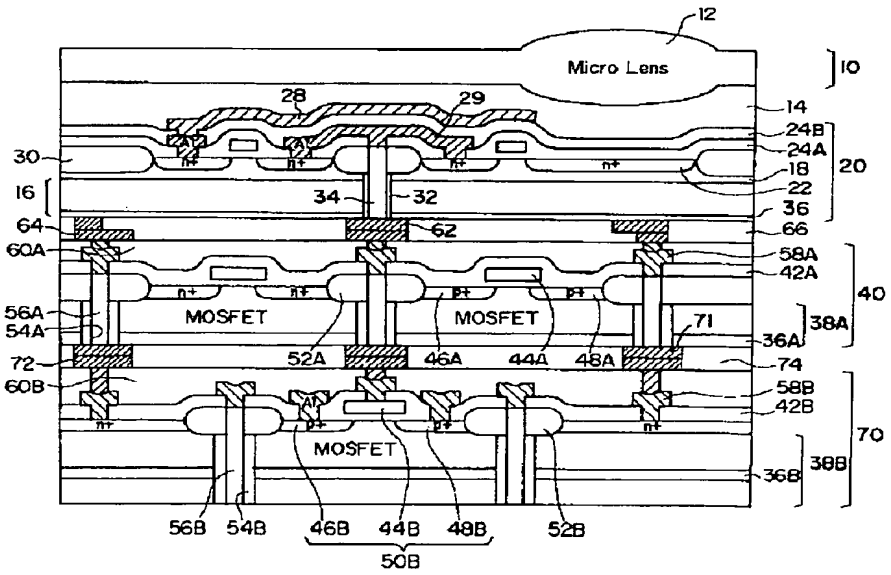
52A
46A
44A
48A
50A

【図５】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MOSFET
MOSFET
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38A
36A
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46A
44A
48A
74
60B
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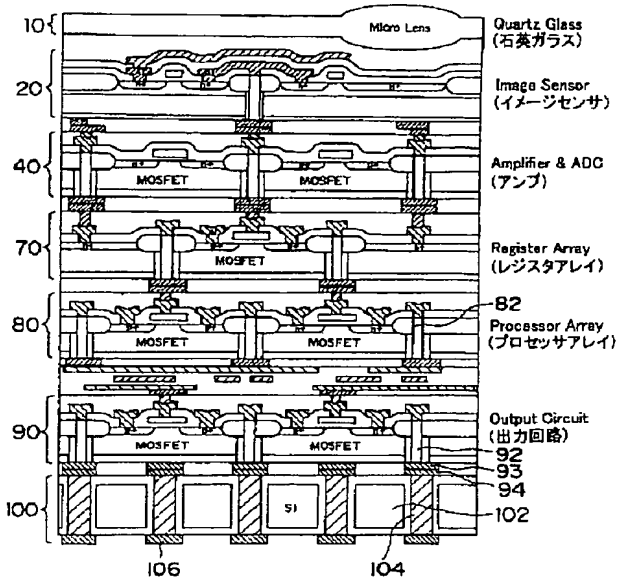
50B

【図６】



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(51)Int.Cl.[7]	識別記号	FI		テーマコード(参考)
H01L	21/8238	H01L	21/90	A　5F110
	27/092		27/08	321G
	27/14		27/14	D
	29/786		29/78	613Z
H04N	5/335			

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Fターム(参考)　4M118 AA10 AB01 BA04 BA14 CA03
EA04 EA20 FA33 GD01 GD04
GD07 HA21 HA33
5B047 BB04 BC01 BC05 DB01
5C024 CY47 EX43 GX03 GY31 HX01
HX17 HX40 HX41
5F033 HH04 HH08 HH11 HH13 HH19
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5F110 AA16 BB10 BB11 CC02 DD03
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